Design and Implementation of a Bias Sequencing Circuit for the HMC463LP5 Low Noise Amplifier

General Description

The HMC463LP5 is a GaAs MMIC PHEMT Low Noise AGC Distributed Amplifier packaged in a leadless 5 x 5 mm surface mount package which operates between 2 and 20 GHz. The amplifier provides 13 dB of gain, 3.0 dB noise figure and 18 dBm of output power at 1 dB gain compression while requiring only 60 mA from a +5V supply. An optional gate bias (Vgg2) is provided to allow Adjustable Gain Control (AGC) of 8 dB typical.

Gain flatness is excellent at ±0.5 dB from 6 – 18 GHz making the HMC463LP5 ideal for EW, ECM RADAR and test equipment applications. The HMC463LP5 LNA I/Os are internally matched to 50 Ohms and are internally DC blocked.

Application

The HMC463LP4 is a distributed amplifier which utilizes the latest Pseudomorphic High Electron Mobility Transistor (PHEMT) technology. The PHEMT transistor is similar to the basic FET transistor which has a gate, drain and source. Like the FET, the gate of the transistor controls the current from the drain to source by applying an electric field which in turn controls the flow of electrons through the channel.   The polarity of the gate control voltage is dependent on the type of device used, which is either N-channel or P-channel. For a P-channel FET, a positive voltage on the gate will cut off current flow from the drain to the source. For the N-channel FET, the opposite is true, a negative voltage on the gate will cut off current flow from the drain to the source. In both cases, 0V will allow for high current flow from the drain to source. The vast majority of amplifiers designed today utilizing FETS use N-channel devices.

Because 0V on the gate result in a high current through the FET, it is important that the gate voltage be applied prior to the drain voltage in order to avoid damage to the device. This is typically accomplished with a "bias-sequencing circuit" which senses for a negative voltage prior to application of a positive voltage to the drain. This product note describes the design and operation of a bias-sequencing network, which is used to control the gate of the HMC463LP4 low noise amplifier.

Application Solution

There are several different topologies which could be utilized to sequence the bias in an amplifier. The topology chosen utilizes few parts and therefore minimizes additional cost to the amplifier stage. Figure 1 shows the schematic of the bias sequencing network as implemented with the HMC463LP4 low noise amplifier. The biasing network is primarily made up of the components D1, Q1 and Q2.   Q2 is a P-Channel MOSFET from International Rectifier and is used to switch the positive voltage in and out of the drain. D1 is a 3.3V zener diode which is used to drop the negative voltage and Q1 is used to apply a negative voltage to the gate of the MOSFET. Resistors R1 and R2 are used to set the proper gate voltage.

Theory of Operation

When -5V is applied to the gate circuit, the zener diode will turn on and pull up the -5V by 3.3V to -1.7V. The base of Q1 is tied to ground through the 10K resistor R4 and therefore turns on when the -1.7V is applied to its emitter. Approximately -1.7V will then be applied to the resistor R5. Since the gate of the MOSFET is high impedance, virtually no current will flow into it, as a result, the majority of the current will flow through R5 and R6 into the 5V supply. The current through resistors R5 and R6 is approximately 0.3mA, resulting in a -3V voltage drop across the resistors. In order to turn on the MOSFET, the Gate to Source (VGS) voltage of Q2 must be much less than the threshold voltage of -0.55V.   Since the voltage drop across the gate to source (VGS) of Q2 is the same as R6 (-3V), Q2 is turned on and 5V is applied to the drain of the HMC463LP5.

When 0V is applied to the gate circuit, D1 and Q1 are off, and the gate of Q2 is pulled up to 5V. VGS is now 0V, which is greater than the threshold voltage of -0.55V. Q2 is off and no voltage is applied to the drain of the HMC463LP5.

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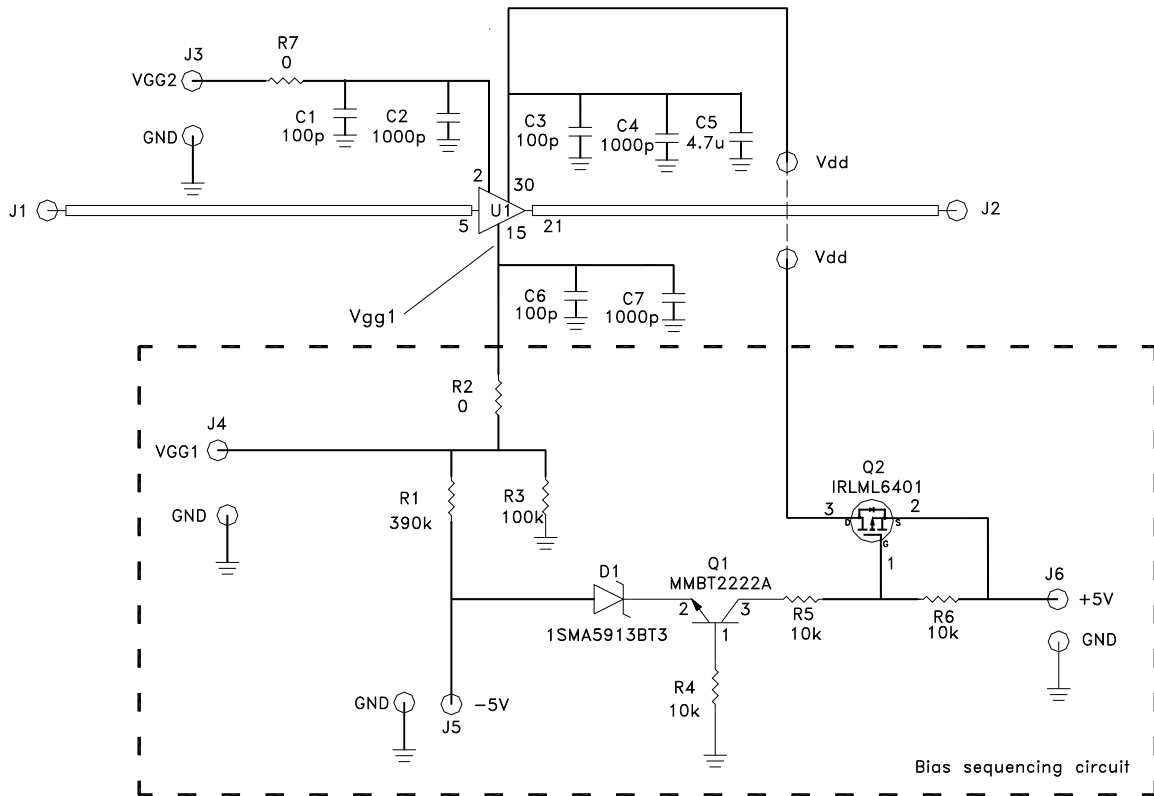
QTY	Designator	Part Number	Vendor	Description
1	U1	HMC463LP5	Hittite Microwave Corp.	GaAs PHEMPT MMIC LNA
1	D1	1SMA5913BT3	ON Semiconductor	3.3V Zener Diode
1	Q1	MMBT2222A	Fairchild Semiconductor	NPN General Purpose Amplifier
1	Q2	IRLML6401	International Rectifier	P-Channel MOSFET
3	C2,C4,C7	ECJ-0EB1H102k	Panasonic	Cap,0402,50V,1000pF
3	C1,C3,C6	ECJ-0EC1H101J	Panasonic	Cap,0402,50V,100pF
1	C5	ECS-T1CY475R	Panasonic	Cap,4.7uF 16V Tant TE Series (Case Size A)
3	R4,R5,R6	ERJ-3GEY10000V	Panasonic	Res,0603,1/16W,10K
2	R2,R7	ERJ-3GSYJ00V	Panasonic	Res,0603,1/16W, 0
1	R1	ERJ-3GEY390KV	Panasonic	Res,0603,1/16W,390K
1	R3	ERJ-3GEY100KV	Panasonic	Resr,0603,1/16W,100K

Figure-1 Bias sequencing network

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Resistors R1 and R3 make up a voltage divider which is used to set the gate voltage to the HMC463L5. The gate voltage is set so that 60mA of drain current is obtained when 5V is applied to Vdd. It was determined that -1V on the gate of the HMC463LP5 will set the drain current to the required value. To achieve this, R1 is set to 390K and R3 to 100K .

Simulated Results
The bias sequence circuit was modeled and then simulated using a spice simulator[1]. Figure 2 shows the results of the simulation. The top trace is the applied voltage to the -5V pin (J5) of the bias sequence circuit. The voltage goes from 0V to -5V at a 1 KHz rate. The second trace is the output of the bias sequence circuit which goes to the Vdd pin (pin 30) of the HMC463LP5. As expected, when there is no voltage applied to J5 the output to Vdd is 0V and when J5 goes to -5V the output to Vdd goes to 5V.
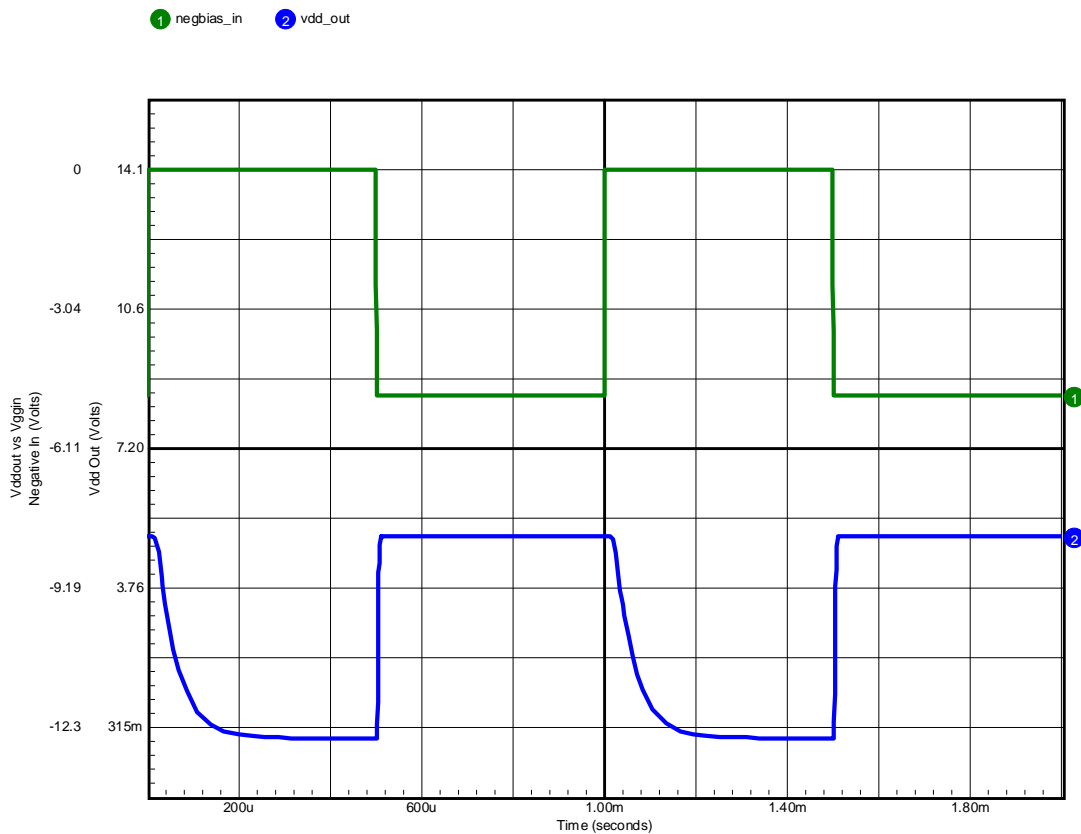

Figure-2 Simulated response of bias sequence circuit

When Vdd goes from 5V to 0V the fall time is approximately 98uSec due to the RC time constant associated with the decoupling capacitors on the Vdd line and the finite resistance in the discharge path. A faster switching time can be achieved by reducing the value of the decoupling capacitors on the Vdd line. The amount of decoupling reduced is dependent on the required amount of noise suppression on the Vdd line and the stability of the

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amplifier. It may also be necessary to use a faster MOSFET (Q2) or transistor (Q1). Figure 3 shows the result when the 4.7uF decoupling capacitor is reduced to 0.01uF.
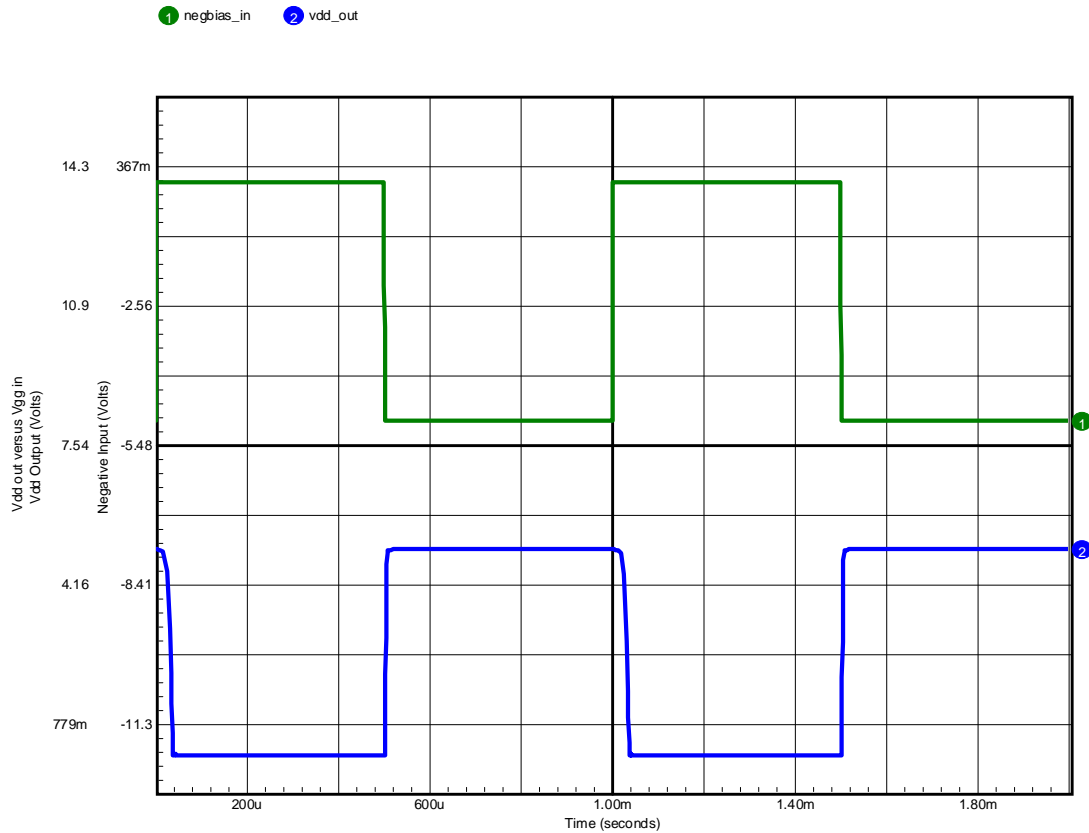

Figure-3 Improved switching speed when values of decoupling capacitors are reduced

This particular bias sequence network requires a minimum negative voltage applied to it in order to function properly. Figure 4 shows a simulation Vdd out versus the input negative voltage. The negative voltage is varied from -5V to 0V. The plot shows that at around -4V, the Vdd output begins to drop due to the MOSFET Q2 beginning to turn off. The bias sequence network can be adjusted to accommodate higher (more positive)voltages (> -4V) by either replacing (or removing) the zener diode with one of a lower break down voltage. If a lower voltage (< -5V) is being applied, then a zener diode with a higher break down voltage should be used.

The P-channel MOSFET being used is sufficient for use with the majority of Hittite amplifiers requiring a bias sequencing network. If the bias-sequencing network is being used to sequence more than one device, then it may be necessary to choose a device, which is capable of handling the higher current requirement. In addition, application of drain voltages greater than 9V should be avoided since it may damage the HMC463LP5. The Hittite datasheet should be referred to for operating conditions of other amplifiers.

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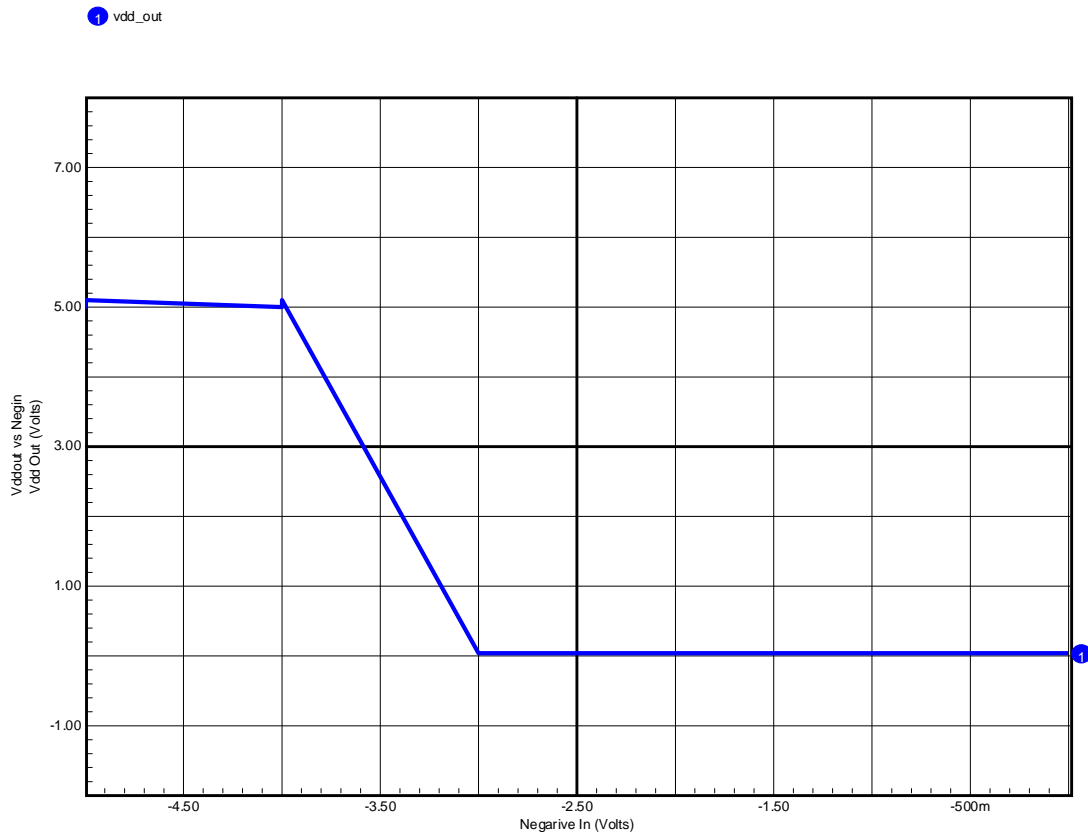

Figure-4 Vdd out versus negative voltage in

Measured Results

To verify the performance of the bias sequence circuit, it was implemented onto a HMC363LP4 evaluation board and tested. Figure 5 shows the evaluation board used with the bias sequence network incorporated. The board is 4 layers. The top layer contains the RF and bias sequencing circuitry and traces. The second layer is separated by 10 mil of Rogers 4350 dielectric material and provides the RF ground plane. Layer 3 is used to route Vdd from the output of the bias sequence circuit to the Vdd input of the HMC463LP4 amplifier. Layer four is not used and is separated by FR4 material. The 4th layer is primarily used for mechanical support.

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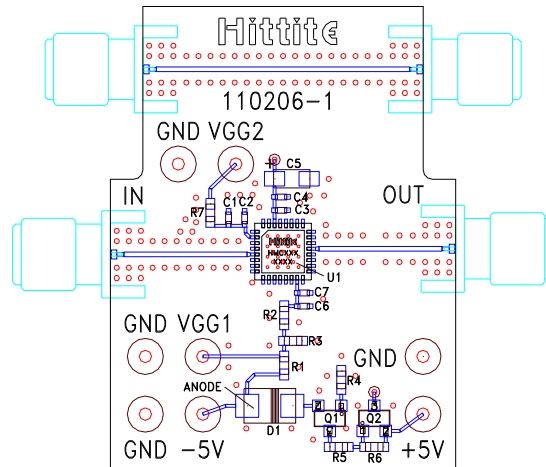

Figure-5 Bias sequence circuit evaluation board

Like the simulation, a 1 KHz square wave varying from 0V to -5V was applied to the negative supply (J5) while a static 5V was applied to the positive supply side of bias sequencing circuit. Using an oscilloscope, the Vgg voltage was measured along with the Vdd voltage inputted into the HMC463LP4 amplifier. The results are shown in figure 6. Like the simulated outcome, the measured results show that when Vdd equals 0V, the negative voltage is 0V and that the fall time of the Vdd input from 5V to 0V is approximately 98uSec when a 4.7uF decoupling capacitor is used on the Vdd line. A noticeable improvement is observed when the 4.7uF decoupling capacitor is reduced to 0.01uF.
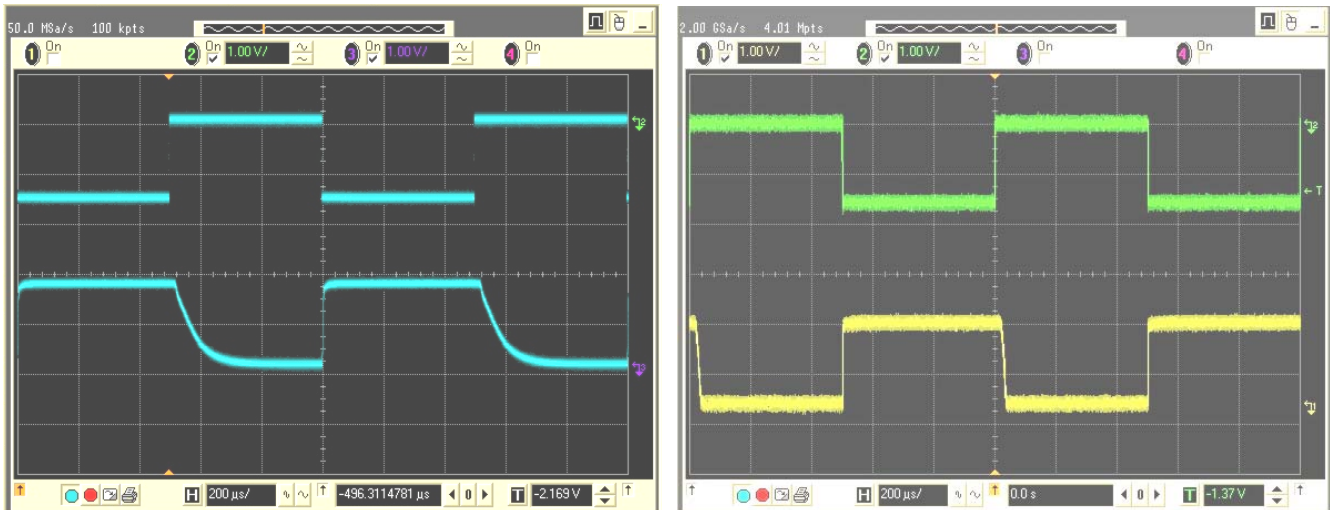
With 4.7uF decoupling Capacitor

With .01uF decoupling capacitor

Figure-6 Measured response of the bias sequence circuit

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Conclusions

A bias-sequencing network was designed, simulated, and implemented onto a HMC463LP5 evaluation board. The circuit prevents positive voltage from being applied to the drain of an amplifier prior to the application of a negative voltage to the gate therefore protecting the amplifier from damage. It has also been shown that the fall time of Vdd from 5V to 0V is the result of the RC time constant of the decoupling capacitors located on the Vdd line and that this fall time can be improved by decreasing the value of the decoupling capacitance.

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[1] ICAP/4 Spice Simulator, Intusoft Corporation, Gardena, CA